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The diagram illustrates a computer system architecture with the following components and connections:

- MEMORY ARRAY 1**: Located at the top, connected to **ROW LINES** and **COLUMN DECODE LINES**.
- STORAGE ARRAY 2**: Two instances, one in the upper middle and one at the bottom, connected to **ROW LINES** and **COLUMN DECODE LINES**.
- I/O LIZING 8**: A central block connected to **ROW LINES** and **COLUMN DECODE LINES**.
- SENSE AMP CIRCUITRY 7**: A block containing a **SENSE AMP** and **SHIFT REGISTER 20**, connected to **ROW LINES** and **COLUMN DECODE LINES**.
- SHIFT LOC**: A block connected to **ROW LINES** and **COLUMN DECODE LINES**.
- SHIFT REGISTER 20**: A detailed circuit diagram showing internal components like **56**, **57**, **58**, **59**, **60**, **61**, **62**, **63**, **64**, **65**, **66**, **67**, **68**, **69**, **70**, **71**, **72**, **73**, **74**, **75**, **76**, **77**, **78**, **79**, **80**, **81**, **82**, **83**, **84**, **85**, **86**, **87**, **88**, **89**, **90**, **91**, **92**, **93**, **94**, **95**, **96**, **97**, **98**, **99**, **100**, **101**, **102**, **103**, **104**, **105**, **106**, **107**, **108**, **109**, **110**, **111**, **112**, **113**, **114**, **115**, **116**, **117**, **118**, **119**, **120**, **121**, **122**, **123**, **124**, **125**, **126**, **127**, **128**, **129**, **130**, **131**, **132**, **133**, **134**, **135**, **136**, **137**, **138**, **139**, **140**, **141**, **142**, **143**, **144**, **145**, **146**, **147**, **148**, **149**, **150**, **151**, **152**, **153**, **154**, **155**, **156**, **157**, **158**, **159**, **160**, **161**, **162**, **163**, **164**, **165**, **166**, **167**, **168**, **169**, **170**, **171**, **172**, **173**, **174**, **175**, **176**, **177**, **178**, **179**, **180**, **181**, **182**, **183**, **184**, **185**, **186**, **187**, **188**, **189**, **190**, **191**, **192**, **193**, **194**, **195**, **196**, **197**, **198**, **199**, **200**, **201**, **202**, **203**, **204**, **205**, **206**, **207**, **208**, **209**, **210**, **211**, **212**, **213**, **214**, **215**, **216**, **217**, **218**, **219**, **220**, **221**, **222**, **223**, **224**, **225**, **226**, **227**, **228**, **229**, **230**, **231**, **232**, **233**, **234**, **235**, **236**, **237**, **238**, **239**, **240**, **241**, **242**, **243**, **244**, **245**, **246**, **247**, **248**, **249**, **250**, **251**, **252**, **253**, **254**, **255**, **256**, **257**, **258**, **259**, **260**, **261**, **262**, **263**, **264**, **265**, **266**, **267**, **268**, **269**, **270**, **271**, **272**, **273**, **274**, **275**, **276**, **277**, **278**, **279**, **280**, **281**, **282**, **283**, **284**, **285**, **286**, **287**, **288**, **289**, **290**, **291**, **292**, **293**, **294**, **295**, **296**, **297**, **298**, **299**, **300**, **301**, **302**, **303**, **304**, **305**, **306**, **307**, **308**, **309**, **310**, **311**, **312**, **313**, **314**, **315**, **316**, **317**, **318**, **319**, **320**, **321**, **322**, **323**, **324**, **325**, **326**, **327**, **328**, **329**, **330**, **331**, **332**, **333**, **334**, **335**, **336**, **337**, **338**, **339**, **340**, **341**, **342**, **343**, **344**, **345**, **346**, **347**, **348**, **349**, **350**, **351**, **352**, **353**, **354**, **355**, **356**, **357**, **358**, **359**, **360**, **361**, **362**, **363**, **364**, **365**, **366**, **367**, **368**, **369**, **370**, **371**, **372**, **373**, **374**, **375**, **376**, **377**, **378**, **379**, **380**, **381**, **382**, **383**, **384**, **385**, **386**, **387**, **388**, **389**, **390**, **391**, **392**, **393**, **394**, **395**, **396**, **397**, **398**, **399**, **400**, **401**, **402**, **403**, **404**, **405**, **406**, **407**, **408**, **409**, **410**, **411**, **412**, **413**, **414**, **415**, **416**, **417**, **418**, **419**, **420**, **421**, **422**, **423**, **424**, **425**, **426**, **427**, **428**, **429**, **430**, **431**, **432**, **433**, **434**, **435**, **436**, **437**, **438**, **439**, **440**, **441**, **442**, **443**, **444**, **445**, **446**, **447**, **448**, **449**, **450**, **451**, **452**, **453**, **454**, **455**, **456**, **457**, **458**, **459**, **460**, **461**, **462**, **463**, **464**, **465**, **466**, **467**, **468**, **469**, **470**, **471**, **472**, **473**, **474**, **475**, **476**, **477**, **478**, **479**, **480**, **481**, **4**

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RANDOM ACCESS MEMORY SYSTEM HAVING  
HIGH-SPEED SERIAL DATA PATHS

Background of the Invention

5           This invention relates to a random access memory comprising a storage array of memory elements arranged in rows and columns, and a plurality of bit lines arranged such that each bit line runs parallel to a respective one of the columns and is connected to at least one of the  
10 memory elements in the respective one of the columns.

          In the area of digital signal processing, random access memories (RAMs) have been used for years as a means of storing digital data. A typical integrated circuit RAM contains a memory array, circuitry—typically row and  
15 column decoders—which addresses selected memory elements, or locations, within that array, and input/output circuitry. The memory array contains a plurality of intersecting row and column lines arranged in a grid. One memory element, capable of holding, for example, one bit of  
20 information, is provided at the point of intersection of every row and column line.

          Memory elements can be classified as either static or dynamic. Dynamic memory elements are those in which the value of any data stored therein slowly decays  
25 with time. To preserve the stored data for an indefinite time, each dynamic memory element must be periodically read and its contents written back with the same data. This process is known as refresh. Static memory elements, on the other hand, are those capable of storing data for an  
30 indefinite period of time without refresh.

          To access information stored within a RAM, a portion of an address supplied to the memory is applied to the row decoder. In response to this portion, the row decoder selectively energizes a particular one of the  
35 plurality of row (or word) lines. Each bit in a resulting accessed row is then read onto a respective column (or bit)



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line. A sense amplifier connected to each bit line detects the level of the bit present on that line, and amplifies it to a higher level. In the case of a RAM comprised of dynamic memory elements, the resulting amplified bit is then applied to the same bit line in order to facilitate refresh. In response to the remainder of the address, the column decoder in conjunction with the input/output circuitry applies the amplified bit present on a selected one of the bit lines to the memory output.

10 Over the past few years, a variety of RAM technologies have been developed, e.g., RAMs containing bipolar memory elements and those containing metal oxide semiconductor (MOS) elements. The former have significantly faster access speeds than the latter.

15 However, bipolar based memories consume a relatively large amount of power, contain relatively few locations per chip, and are expensive. Advantageously, MOS RAMs not only consume far less power, but also can be provided at a much lower price than bipolar. Moreover, recent developments in

20 the design of digital integrated circuits have led to significant decreases in the physical size of individual MOS memory elements, and correspondingly have provided significant increases in the storage capacity of individual MOS RAM chips. Consequently, the number of MOS memory

25 chips required to implement a memory system of given storage capacity, i.e., the "chip count," has significantly decreased.

However, various physical constraints on the design of MOS RAMs, for example, substantial internal

30 capacitances and limited number of terminals which can be connected to a chip, have generally prevented the bandwidth of a MOS RAM, i.e., the amount of data that can be transferred into or out of the memory chip per unit time, from being increased. Consequently, decreasing the chip

35 count of an MOS based memory system of given storage capacity causes a reduction in the overall bandwidth. Thus, in those applications where the operating speed of



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the digital system is primarily determined by memory bandwidth, e.g., video frame stores, use of relatively inexpensive, high capacity MOS RAMs is no longer being favored over more expensive, less dense RAMs.

5 Various approaches aimed at increasing the bandwidth of a MOS RAM have been disclosed in the art. In particular, U. S. patent 4,106,109, teaches that the access rate of a multi-array MOS RAM can be increased by storing the bit produced by each array during a memory read  
10 operation in a separate register, positioned external to the memory arrays, prior to applying these bits to the output circuitry. Disadvantageously, this arrangement only increases access speed during a memory read operation and requires a significant amount of area on the integrated  
15 circuit for routing the leads connecting the register to the existing memory circuitry. Alternatively, U. S. patent 4,144,590, teaches that access speed can be increased by amplifying the output signal of each sense amplifier prior to applying it to a respective bit line. However, while  
20 this arrangement requires a small amount of additional circuitry, the increase in access speed produced thereby is insufficient to overcome the bandwidth limitation in a typical high-capacity, low chip-count MOS based memory system.

The problem is solved in accordance with the  
25 invention in a random access memory in which the memory further comprises a shift register positioned substantially parallel to at least one of the rows and connected to at least one of the bit lines whereby a row of data can be transferred to and from the memory at a rate substantially  
30 faster than the single-bit access rate of the memory.

#### Summary of the Invention

In accordance with the present invention, the bandwidth of an integrated circuit RAM is increased, while requiring a minimal amount of additional on-chip circuitry,  
35 and while retaining its random access capability, by disposing a shift register within the memory array such that the shift register lies substantially parallel to the



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memory element rows and is connected to at least individual ones of the bit lines. Once a word line is energized, and the amplified bits are provided on each bit line, those bits are applied not only to the input/output circuitry, but also to respective locations in the shift register. The bits can thereafter be read out of the register as a serial data stream at a rate substantially higher than the single-bit random access rate. Writing is accomplished by serially applying the input bits to the shift register and subsequently applying these bits in parallel from the shift register to the respective bit lines, whence they are written into a selected row. The invention thus provides the ability to concurrently transfer a row of bits to and from the random access memory.

The above-described structure allows a row of bits to be transferred to or from the memory array within the time required for one conventional random memory access. This information can then be read out at a rate limited only by the speed of the shift register. Advantageously, then, a substantial increase in access speed and bandwidth results over that obtainable with prior art MOS RAMs.

In preferred embodiments of the invention, the shift register is positioned so as to be intersected by the bit lines, thereby requiring minimal amount of lead routing between the register and the bit lines. Consequently, this arrangement is advantageously simple and inexpensive to implement.

As a result, MOS RAMs and high capacity, low chip count MOS RAM based memory systems incorporating the teachings of this invention may advantageously be used in applications heretofore reserved for expensive, less dense technologies.

#### Brief Description of the Drawing

The invention may be clearly understood from a consideration of the following detailed description and accompanying drawing in which:



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FIG. 1 is a block diagram of a random access memory (RAM);

FIG. 2 is a block diagram of a memory array used in the memory of FIG. 1 which, more particularly, incorporates the teachings of the present invention;

FIG. 3 is a diagram showing the timing relationships between the various control signals needed to shift data bits through a shift register used in the memory array of FIG. 2;

FIG. 4 is a diagram showing the timing relationships between the various control signals needed to simultaneously transfer data bits stored within the shift register into a selected row within the memory array; and

FIG. 5 is a diagram showing the timing relationships between the various control signals required to transfer all the data bits from a selected row of the memory array into respective locations of the shift register.

#### Detailed Description

FIG. 1 depicts a block diagram of a random access memory (RAM). The RAM includes a memory array 1 having a plurality of addressable memory elements arranged in intersecting rows and columns. Illustratively, each memory element is capable of storing one bit of data. As described below, memory array 1 incorporates the teachings of the present invention. Also included in the RAM are row decoder 5, column decoder 13, input/output buffer 11 and clock generator 15. These latter blocks are all of conventional construction and are well known to RAM designers.

To read the data bit stored within a particular memory element, a binary address of that element is externally supplied to the RAM via the ADDRESS IN pins and extended to the decoder circuitry by address bus 17. In addition, a high to low level transition is applied to pin RAS (Read Address Strobe). Clock generator 15 responds to this transition by applying a clock signal to row decoder 5



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via lead 26. Row decoder 5, in turn, responds to this clock signal and a portion of the address present on address bus 17 to energize one of word lines 3 corresponding to that address portion. Subsequently, in response to a high to low level transition applied to pin CAS (Column Address Strobe), clock generator 15 applies a clock signal to column decoder 13 via lead 24. Column decoder 13, in turn, responds to this signal and to the remainder of the address present on address bus 17 to energize one of the column decode lines 10 corresponding to that address portion. The bit stored within the memory element lying at the intersection of the selected row and column is then applied by the circuitry within memory array 1, via input/output line 8, to input/output buffer 11, wherein the bit is temporarily stored. Shortly thereafter, clock generator 15, via lead 23, signals input/output buffer 11 to apply its contents, as the memory's output, to output pin DATA OUT.

Writing is accomplished by substantially the reverse process. In particular, an input data bit is applied to pin DATA IN, and the desired address of that data bit is externally applied to the RAM through the ADDRESS IN pins. This is followed by high to low level transitions on input pins WE (Write Enable) and RAS, followed after a predetermined period of time by a similar transition applied to pin CAS.

FIG. 2 is a block diagram of memory array 1 (shown in FIG. 1) which incorporates the teachings of the present invention. Memory array 1 is illustratively comprised of two separate storage arrays 2. Each storage array contains half of the above-mentioned addressable word lines 3 and n bit lines 4, the word and bit lines being arranged in an intersecting grid. A memory element, e.g., memory element 32, lies at the intersection of each word and bit line within each one of storage arrays 2. In particular, this memory element is comprised of MOS transistor 38 and capacitor 40. A data bit of value "1",

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for example, is stored within this memory element as the presence of a small quantity of electrical charge stored in capacitor 40.

Sense amplifier circuitry 7 and input/output gating 9 are centrally positioned between storage arrays 2 and are connected to every bit line within memory array 1. Circuitry 7 includes sense amplifiers 33a-33n, illustrative basic circuitry of sense amplifier 33n being explicitly shown. Circuitry 7, and clock signals A, B and C which control it, are both well known in the art, and as such will not be described. See, for example, Memory Data Book and Designer Guide, pages 236-238 published by the Mostek Corporation.

To read the data bit stored within memory element 32, for example, the associated one of word lines 3—word line 30—is energized by row decoder 5 as previously described. This causes the transistor in each memory element on word line 30 and, in particular, transistor 38, to conduct. If a "1" was previously stored within, for example, memory element 32, the charge existing within capacitor 40 is thereby transferred via transistor 38 to the associated one of bit lines 4—bit line 31. If a "0" was previously stored in this memory element, capacitor 40 will contain no charge, and none will be transferred to the bit line.

Assume, in particular, that a "1" has been stored in memory element 32. The charge transferred from memory element 32 to bit line 31 will generate a small voltage, for example, on the order of several hundred millivolts, on this bit line because the capacitance associated with bit line 31 is substantially greater than that of capacitor 40. To accurately detect this voltage, sense amplifier 33n receives a reference voltage present on another one of bit lines 4—bit line 34. The latter voltage is approximately midway between two extremes of voltage expected on bit line 31 resulting from memory element 40 being either in a charged or discharged condition and is produced by a dummy



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memory element (not shown) located on bit line 34. This dummy memory element is read whenever a memory element connected to bit line 31 is read. (Voltages produced by dummy memory elements located on each of the other upper  
5 bit lines are, at the same time, read onto their respective bit lines.) Sense amplifier 33n hereafter differentially amplifies the signals present on bit lines 31 and 34 and applies the resulting amplified data bit to these same bit lines. This latter operation preserves the data bit in  
10 memory element 32 in that it replenishes the stored charge previously taken from that element. This operation is commonly known as "refreshing".

In addition, the amplified data bit on bit line 34 is received by transistor 35n within input/output  
15 gating 9. As previously described, a column decode signal from column decoder 13 is thereafter applied to one of column decode lines 10. This signal, received at the gate of transistor 35n, causes transistor 35 to conduct and thereby transfer the signal present on bit line 34 to  
20 input/output line 8.

To write into memory element 32, a process using a data path essentially the reverse of that described above is used. In particular, an input data bit, for example a "1", is applied to input/output line 8. A column decode  
25 signal from column decoder 13 is applied to transistor 35n causing it to transfer the data bit on input/output line 8 to sense amplifier 33n via bit line 34. Concurrently, word line 30 is energized causing transistor 38 within memory element 32 to conduct. Sense amplifier 33n, in response to  
30 clock signals produced by clock generator 15, amplifies the input data bit and subsequently applies it to bit line 31. From there, conducting transistor 38 routes the data bit into memory element 40 wherein this bit value is preserved as a stored charge. On the other hand, if the value of  
35 this input data bit had been a "0", memory element 40 would be discharged.



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Over the last few years, changing techniques of MOS design and manufacture have produced significant decreases in the physical size of individual MOS memory elements, e.g., element 32. This has dramatically increased the number of memory elements that can comprise a single memory array of a given chip area. As a result, the number of MOS memory chips required to implement a memory system has significantly decreased. However, various physical constraints on the design of MOS RAMS, for example, substantial internal capacitances and limited number of terminals on a chip, have generally prevented the bandwidth of a MOS RAM, i.e., the amount of data that can be transferred into or out of the memory chip per unit time, from being increased. Consequently, decreasing the chip count of an MOS based memory system causes a reduction in the overall bandwidth. Thus, the use of high density MOS RAMs has been limited in those applications e.g., video frame stores, where the operating speed of the system is primarily determined by the memory bandwidth.

The present invention is directed to an arrangement for providing a RAM with a substantially increased bandwidth while (a) minimizing the need for additional circuitry and chip area and (b) retaining its random access capability. In accordance with the invention, this is achieved by disposing a shift register within the memory array such that it lies parallel to the word lines and is connected to at least some of the bit lines. High-speed serial input and output lines are provided by the shift register and operate independently of the slower speed input and output lines normally provided by the RAM.

Through this arrangement, a row of data bits can be either written into or read from the memory array at high-speed. In particular, to write a row of data bits into the memory array, these data bits are first applied as a high-speed data stream to the serial input line. Once stored within the shift register, all the bits comprising



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the row are simultaneously applied to respective bit lines through which they are routed to and stored within a previously accessed row. Alternatively, to read an accessed row, all the bits comprising that row are first  
5 simultaneously read from the memory and stored in respective locations within the shift register. Thereafter, they are shifted out of the shift register and applied to the serial output line as a high-speed serial bit stream. Thus, through this arrangement, a row of data  
10 bits can be transferred either into or out of the memory array in the time required for one single bit random memory access and then serially shifted out at high speed.

As a result of its substantially increased bandwidth, this arrangement can be advantageously used in  
15 any system wherein operating speed is predominantly determined by memory bandwidth. One such application is video frame store memories. In particular, each row of bits within the RAM can correspond to one line of information on a video display, e.g., cathode ray tube,  
20 terminal. With this arrangement, a line of information can be transferred between the frame store memory and the display in considerably less time than would be required to access the line conventionally, i.e., randomly accessing each location comprising that line. Consequently, this  
25 will significantly reduce the time required to refresh the display and will thereby significantly increase the operating speed of the system. At the same time, the fact that the random access capability of the memory is retained means that the stored video image can be efficiently  
30 updated. In addition, since only one random access is required to display each line of video information, the rest of the random access memory bandwidth is available for updating the display.

In the present illustrative embodiment, in  
35 particular, shift register 20 is oriented parallel to word lines 3 and is located in the vicinity of the midpoint of bit lines 4. More particularly, shift register 20 is



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connected to half the bit lines within memory array 1, and, even more particularly, those lines of bit lines 4 which feed the lower one of storage arrays 2. Shift register 20 contains as many shift locations, 50a,...,50n, as there are 5 bit lines connected to the lower one of storage arrays 2. Both the parallel input and output of each storage location is connected to a respective bit line. Additionally, a serial input signal  $SD_{IN}$  from pin  $SD_{IN}$  (Shift Data Input—shown in FIG. 1) is extended via lead 21 to shift 10 register 20 and a serial output signal from shift register 20 is extended via lead 22 to output pin  $SD_{OUT}$  (Shift Data Output—also shown in FIG. 1). Operation of shift register 20 in conjunction with the rest of memory array 1 will now be described.

15 Shift location 50n, for example, is comprised of inverters 53 and 56 and MOS field effect transistors 52, 54, 55 and 57. For the sake of brevity the term "MOS field effect transistors" is hereinafter referred to as either MOS transistor or transistors. Inverters 53 and 56 are 20 comprised of MOS transistors 53a and 56a, respectively, and MOS resistors 53b and 56b, respectively. A data bit is stored in shift location 50n through the presence or absence of a stored charge at the input of both inverters, i.e., the gates of transistors 53a and 56a. Because the 25 input impedance of these transistors is substantial, charge can be retained at these inputs for a relatively long period of time. Transistors 52 and 55 perform the shifting function. The rate of shifting is determined by the frequency of clock signal SH CLK continuously applied to 30 pin SH CLK (Shift Clock—shown in FIG. 1). The rate of this clock signal can be independent of the rate of any other control signal applied to the RAM. Its value need only be sufficiently high to enable all the data bits stored within the shift register to be serially shifted 35 into or out of the register at a rate determined by the desired memory bandwidth.



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In particular, clock generator 15 responds to clock signal SH CLK and produces a non-overlapping two-phase shift clock signal to control the shift function. This clock signal is comprised of phases  $\phi_A$  and  $\phi_B$  which are shown in FIG. 3. A positive pulse occurs on phase  $\phi_A$  followed by a positive pulse on phase  $\phi_B$ . Phase  $\phi_A(\phi_B)$  is applied to the gate of transistor 52 (55). Whenever a pulse on phase  $\phi_A$  occurs, a serial input data bit from serial input signal  $SD_{IN}$  present on lead 21 is transferred to the input of inverter 53 via conducting transistor 52. The input data bit need only be valid during the non-shaded intervals of signal  $SD_{IN}$  as shown in FIG. 3. Inverter 53 inverts the serial input data bit and applies it to the source lead of transistor 55. The following pulse of clock phase  $\phi_B$ , causes transistor 55 to conduct, thereby completing the shift into shift location 50n by transferring the inverted data bit to the input of inverter 56. Thereafter, the original value of the data bit appears at the output of inverter 56 and is applied via lead 58 to the input of the following shift location (not shown).

Throughout shifting, control signal SR EN (Shift Register Enable) remains low. This control signal, when low, signals clock generator 15 that a data transfer operation between the memory array and the shift register is not to be initiated. This causes clock generator 15 to place a low level on control signals  $SR_{READ}$  (Shift Register Read) and  $SR_{LOAD}$  (Shift Register Load)—both of which will be discussed below. This prevents switching transistors 57 and 54 from conducting. The input and output of shift location 50n are thereby disconnected from bit line 31, thus effectively isolating the data stored therein from this bit line. Since a similar operation occurs involving each of the other shift locations, shift register 20 is effectively decoupled from memory array 1. This thus ensures that data can be shifted within shift register 20 not only at a rate solely determined by the frequency of



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signal SH CLK, but, more importantly, without interfering with any random access operation undertaken involving memory array 1.

Once data has been shifted into the shift register 20, the data bits stored in its respective shift locations are simultaneously transferred in parallel to respective ones of bit lines 4. For better understanding, reference should be made throughout the following discussion not only to FIG. 2, but also to FIG. 4, the latter depicting the proper timing relationship among the necessary control signals.

In particular, to initiate a row transfer from the shift register to one of the memory arrays, the level of control signal SR EN is raised after at least a minimum time interval,  $t_{min}$ , has elapsed after the rising edge of clock phase  $\phi_B$ . Any shifts in progress are completed during this interval. During the time that control signal SR EN remains raised, clock generator 15, suspends the normal sequence of clock phases  $\phi_A$  and  $\phi_B$ , thereby precluding, during a row transfer operation, shifting of data among the shift locations of shift register 20. Shortly after the level of control signal SR EN is raised, the level of control signals  $\overline{RAS}$  applied to pin  $\overline{RAS}$  and  $\overline{WE}$  applied to pin  $\overline{WE}$  are lowered. In response to the transition on control signal  $\overline{RAS}$ , the RAM addressing circuitry during interval  $t_1$  accesses a particular row within the memory array. The transition on control signal  $\overline{WE}$  indicates to clock generator 15 that a memory write operation is to be initiated. There is, of course, no need to refresh the accessed row when, as in this instance, data is being transferred into it from the shift register. However, to simplify the circuitry of sense amplifiers 7 and clock generator 15, the refresh operation is automatically evoked whenever a row is accessed, regardless of whether a memory read or write operation is being undertaken. During time interval  $t_2$ , the contents of the accessed row are applied to the bit lines and the locations



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comprising that row are thereafter refreshed by sense amplifiers circuitry 7.

Once the refresh operation is complete, such as at the beginning of time interval  $t_3$ , control signal CAS is lowered. This causes clock generator 15 to produce a pulse on control signal SR<sub>READ</sub>. This pulse causes MOS transistor 57 within shift location 50n and the corresponding transistors in each of the other shift locations of shift register 20 to conduct, thereby transferring the contents of each shift location to the associated bit line. For example, transistor 57 when conducting causes the contents of storage location 50n present on lead 58 to be applied to bit line 31. As a result, the contents of the accessed row in the memory array are over-written by the data bits stored in the shift register.

In addition it will be readily appreciated that with the addition of well-known control circuitry, a single bit could be written, using the memory accessing circuitry, into any location within the accessed row using a bit applied to the DATA IN pin. This operation could be used, for example, to update the value of a particular bit located within the transferred row in the event its value changes from the time the row has been shifted into the shift register and the time the row is transferred into the memory array. At the conclusion of the row transfer and single bit write operations, the level of control signal SR EN is lowered to once again permit shifting to occur.

The data bits comprising a selected row within the memory array can also be simultaneously transferred in parallel from that row to respective locations in the shift register and thereafter shifted out at high speed. The bits shifted out of the shift register comprise the serial output signal SD<sub>OUT</sub>. For better understanding, reference should be made throughout the following discussion, not only to FIG. 2, but also to FIG. 5, the latter depicting the proper timing relationships among the necessary control



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signals.

To initiate this data transfer, as in FIG. 4, the level of control signal SR EN is raised after the previously described interval of time,  $t_{min}$ , has elapsed  
5 after the rising edge of clock phase  $\phi_B$ . Thereafter, the level of control signal  $\overline{RAS}$  is lowered. This initiates a memory read during interval  $t_4$  and subsequent refresh of a selected row of the memory array by sense amplifiers circuitry 7 during interval  $t_5$ . Once the refresh is  
10 complete, control signal  $\overline{CAS}$  is lowered. In response thereto, clock generator 15 produces a positive pulse in both control signal SR LOAD, and clock phase  $\phi_B$ . Together, the effect of these pulses is to transfer the data bit present on each bit line into the corresponding shift  
15 location within shift register 20 during time interval  $t_6$ . For example, the data bit present on bit line 31 is transferred through MOS transistor 54, inverter 53, and MOS transistor 55 to the proper position within shift location 50n, i.e., at the input of inverter 56. Again it  
20 will be readily appreciated that with the addition of well-known circuitry, a single data bit could be read once this row transfer is completed from any location within the accessed row using the memory accessing circuitry. At the conclusion of the row transfer and single bit read  
25 operations, the level of control signal SR EN is lowered to once again permit shifting.

While a preferred embodiment has been described in terms of MOS components, it should be clearly understood that the teachings of the present invention, as will be  
30 obvious to those skilled in the art, are applicable to any memory technology which employs a memory comprised of individual memory elements, as a way of substantially increasing the bandwidth of that memory. Consequently, many and varied arrangements embodying these teachings may  
35 be derived by those skilled in the art without departing from the spirit and scope of the invention.



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Claims

1. A random access memory comprising:  
a storage array of memory elements arranged in rows and columns, and  
5 a plurality of bit lines arranged such that each bit line runs parallel to a respective one of the columns and is connected to at least one of the memory elements in the respective one of the columns  
CHARACTERIZED IN THAT  
10 the memory (1) further comprises:  
a shift register (20) positioned substantially parallel to at least one of the rows (30) and connected to at least one of the bit lines (31) whereby a row of data can be transferred to and from the memory at a rate  
15 substantially faster than the single-bit access rate of the memory.
2. A random access memory in accordance with claim 1  
CHARACTERIZED IN THAT  
20 the memory (1) further comprises:  
circuitry (54, 57, 25) for transferring data between the shift register (20) and the one of the bit lines (31).
3. A random access memory in accordance with  
25 claim 2  
CHARACTERIZED IN THAT  
the circuitry (54, 57, 25) transfers the data in parallel between the shift register (20) and the one of the bit lines (31).
- 30 4. A random access memory in accordance with claims 2 or 3  
CHARACTERIZED IN THAT  
the circuitry (54, 57, 25) applies signals from one of the respective bit lines to a respective shift  
35 location within the shift register (20).
5. A random access memory in accordance with claim 4



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CHARACTERIZED IN THAT

the memory further comprises:

- input circuitry (21, 25) for applying input data  
to the shift register (20) and output circuitry (22, 25)  
5 for receiving output data from the shift register.  
6. A random access memory in accordance with  
claim 5

CHARACTERIZED IN THAT

- the input and output data are streams of serial  
10 data.  
7. A random access memory in accordance with  
claim 5

CHARACTERIZED IN THAT

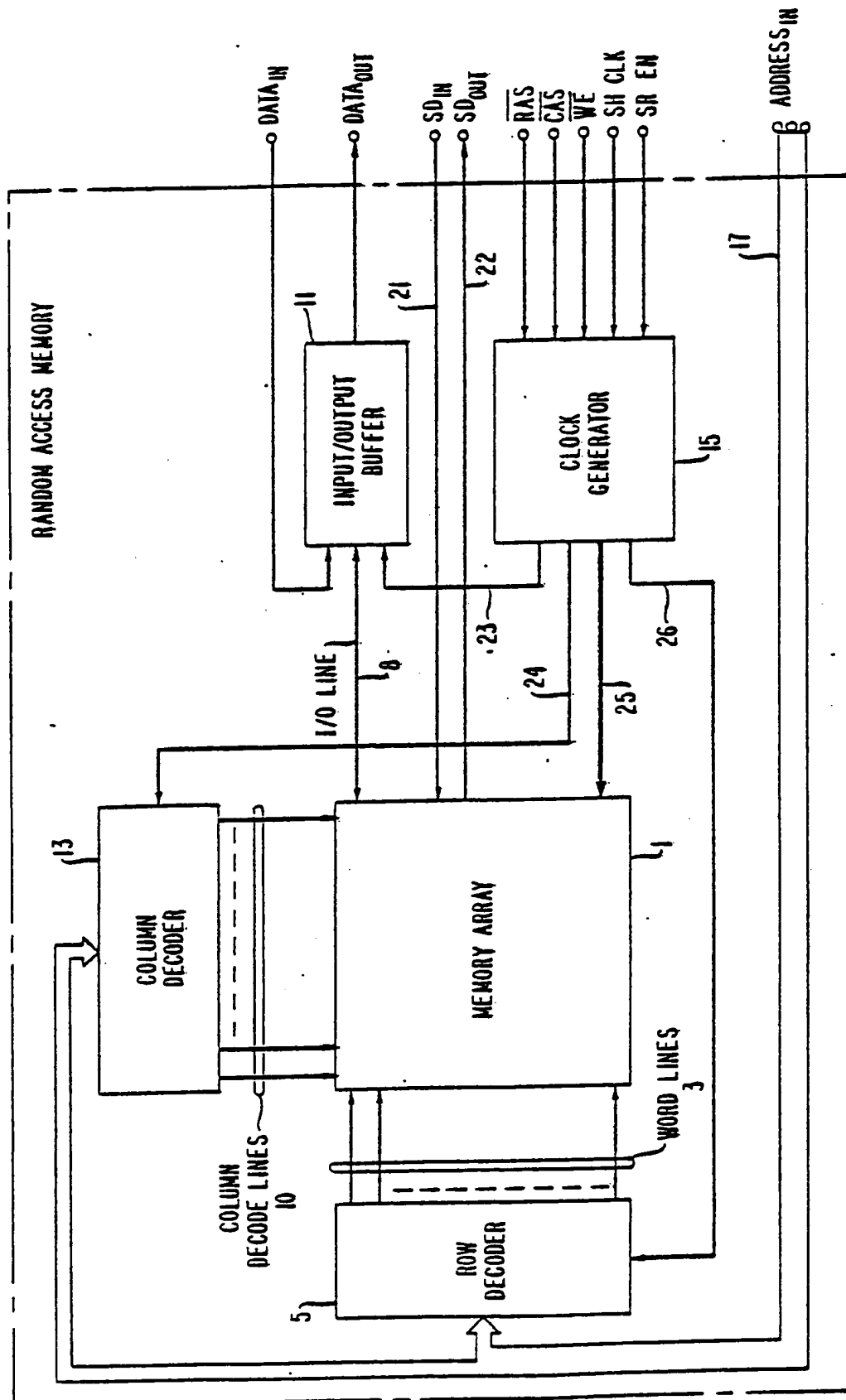
- the memory further comprises:  
15 a sense amplifier circuitry (7) connected to the  
bit lines (4) and wherein the shift register (2) is  
positioned adjacent to the sense amplifier circuitry.  
8. A random access memory in accordance with  
claim 1

20 CHARACTERIZED IN THAT

the shift register (20) is positioned within the  
random access memory (1) such that the shift register  
intersects each one of the bit lines (4) in the vicinity of  
the midpoint of the bit line (4).

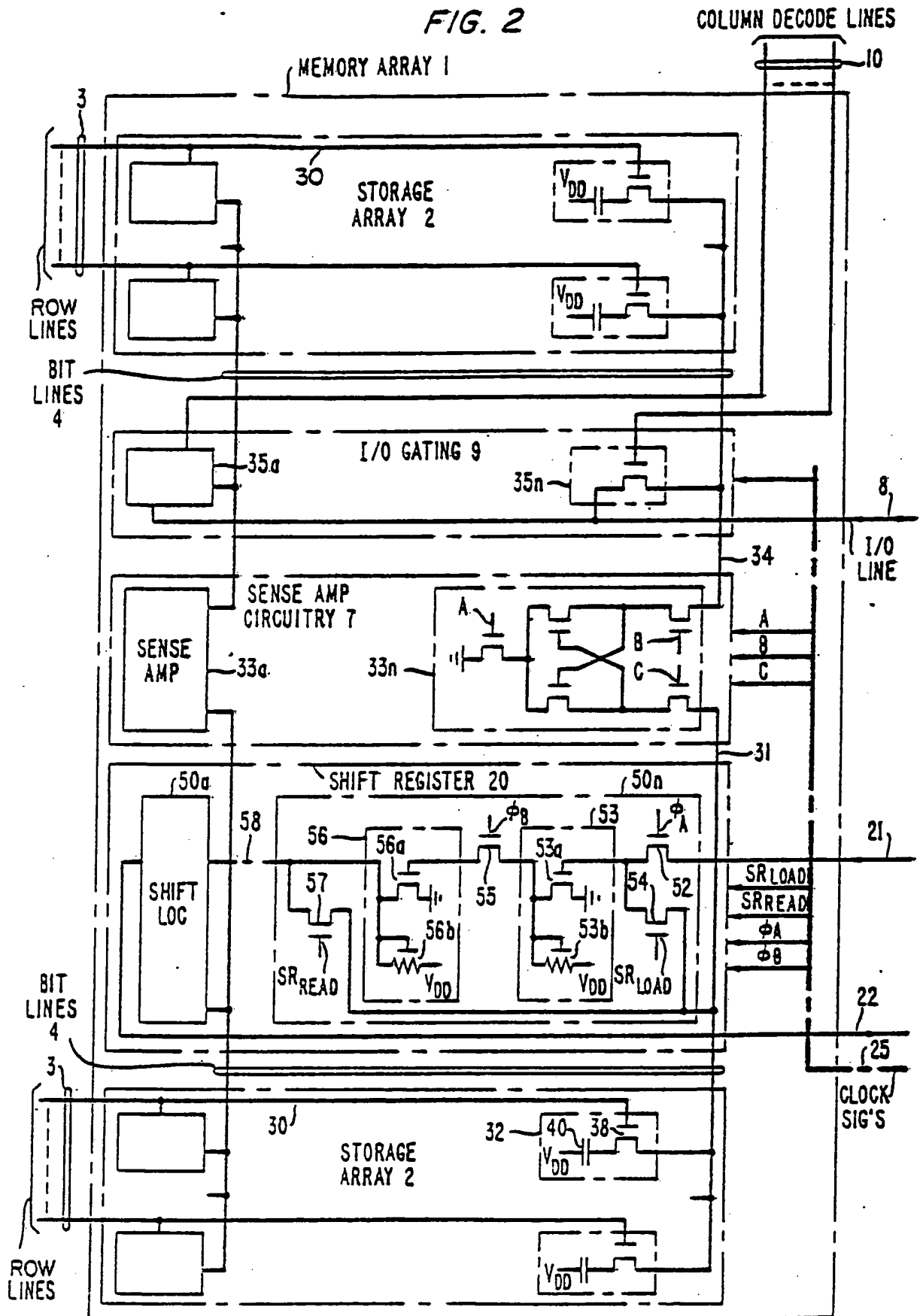


FIG. 1



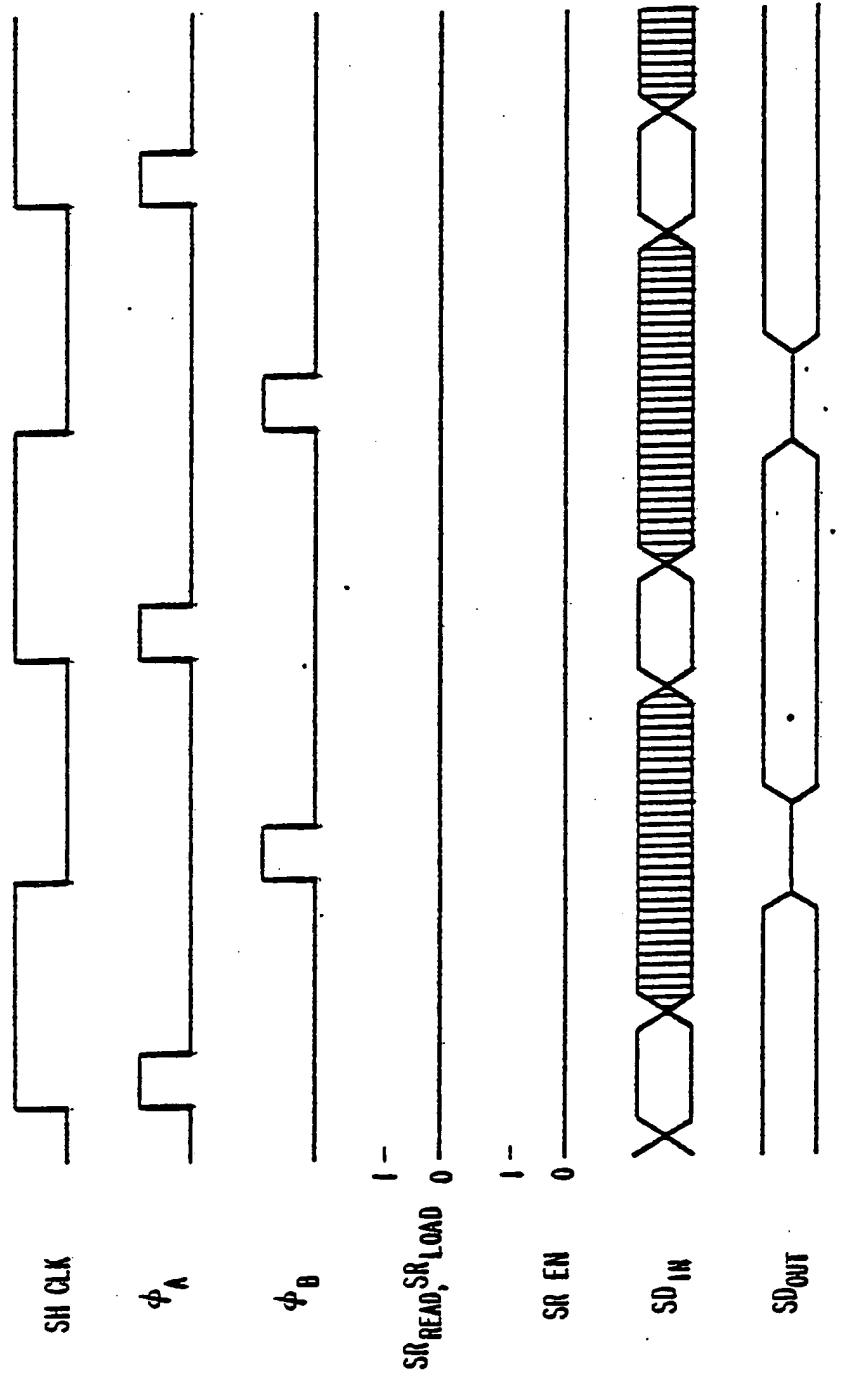
2/5

FIG. 2



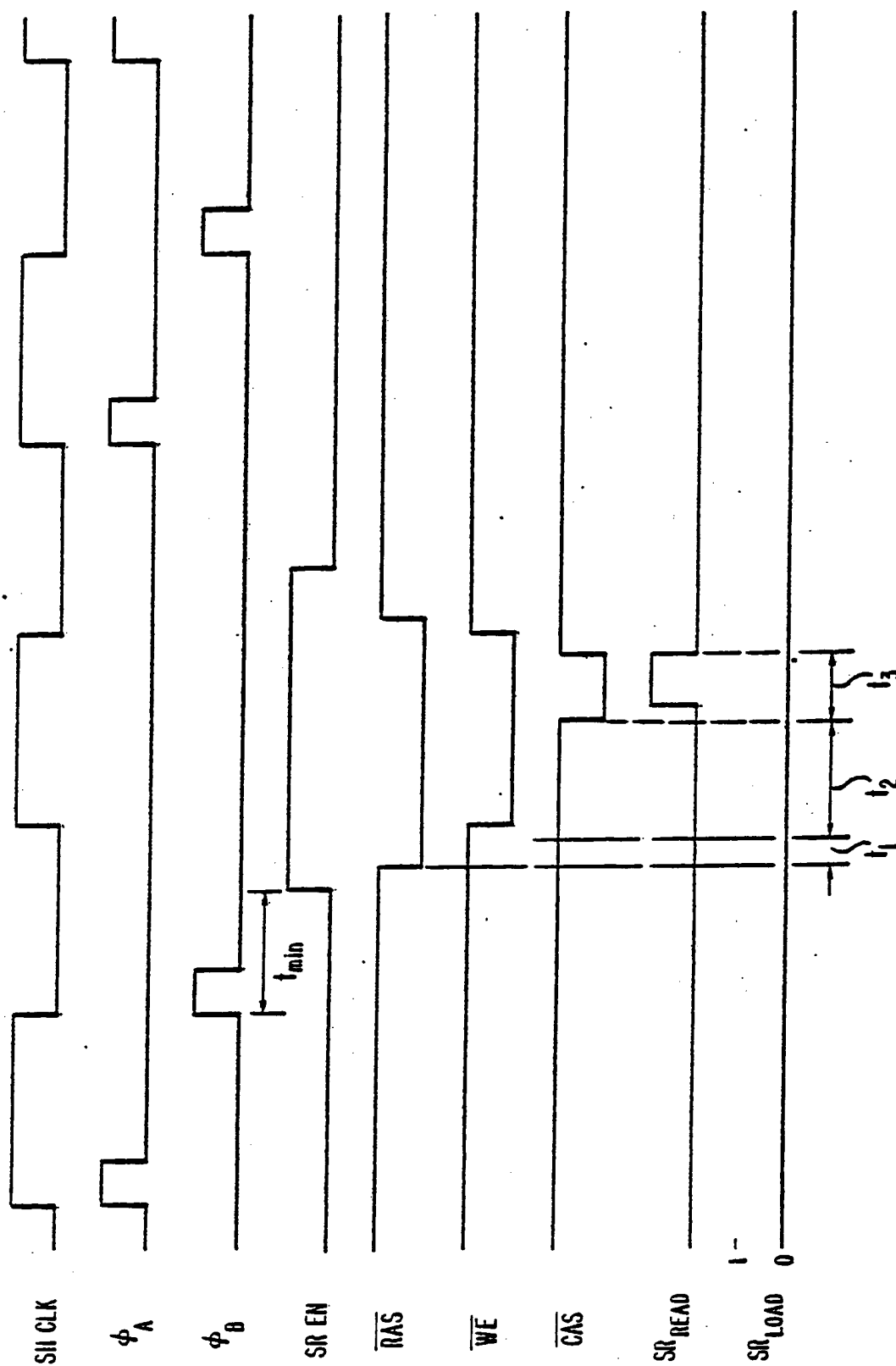
3/5

FIG. 3



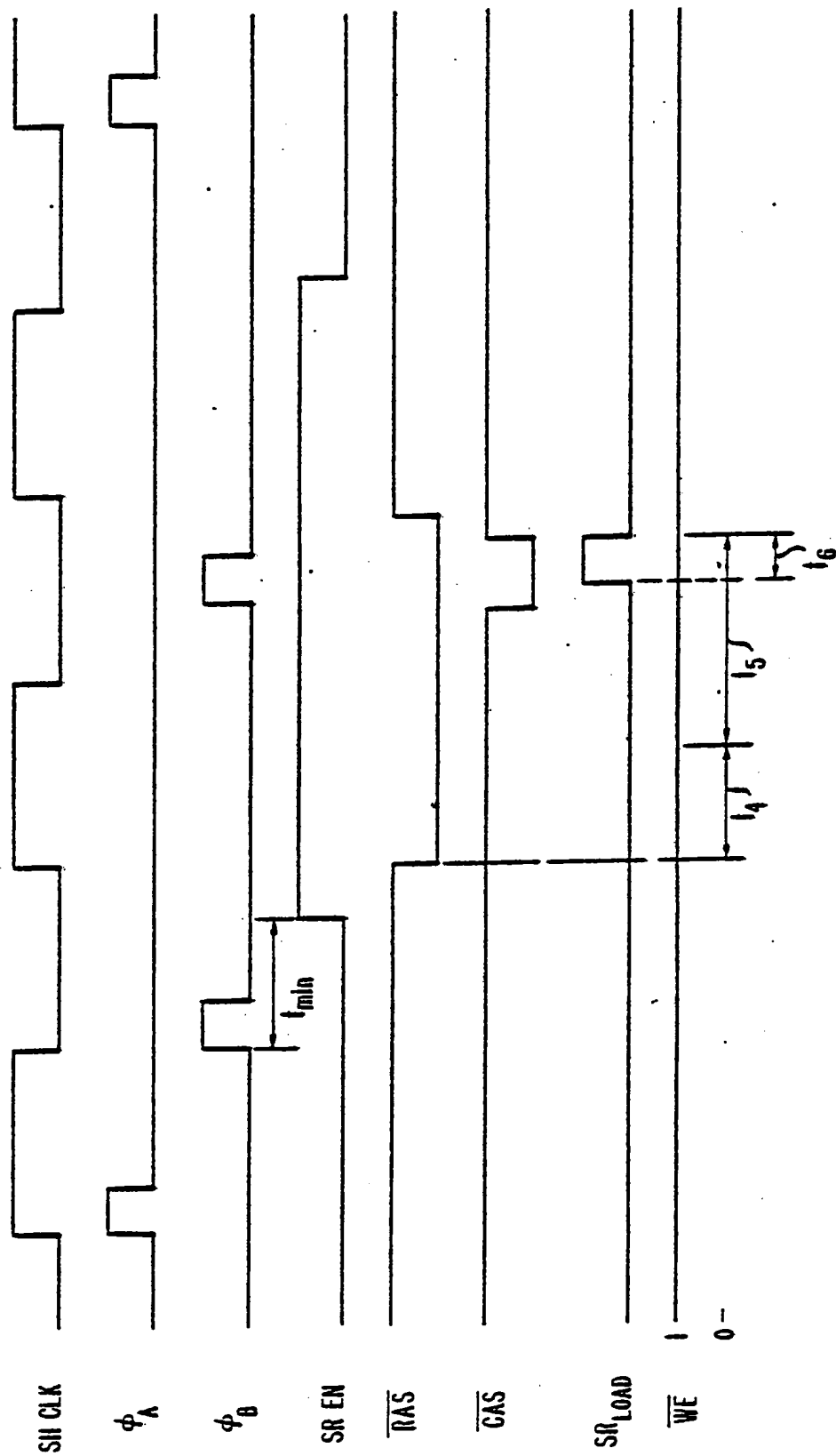
4/5

FIG. 4



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FIG. 5



## INTERNATIONAL SEARCH REPORT

International Application No PCT/US81/01744

<b>I. CLASSIFICATION OF SUBJECT MATTER</b> (If several classification symbols apply, indicate all) *		
According to International Patent Classification (IPC) or to both National Classification and IPC		
INT. CL <sup>3</sup> G11C 7/00, 8/00 U.S. CL. 365/221		
<b>II. FIELDS SEARCHED</b>		
Minimum Documentation Searched *		
Classification System	Classification Symbols	
US	365/205, 221, 240	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched *		
<b>III. DOCUMENTS CONSIDERED TO BE RELEVANT</b> <sup>14</sup>		
Category *	Citation of Document, <sup>15</sup> with indication, where appropriate, of the relevant passages <sup>17</sup>	Relevant to Claim No. <sup>16</sup>
X	US, A, 4,044,339, Published 23 August 1977, Robert O. Berg.	1-6
X	US, A, 3,930,239, Published 30 December 1975, Roelof Herman Willem Salters et al.	7
A	US, A, 3,914,750, Published 21 October 1975, David R. Hadden, Jr.	
A	US, A, 3,771,147, Published 06 November 1973 Harry Joseph Boll et al.	
<p>* Special categories of cited documents: <sup>18</sup></p> <p>"A" document defining the general state of the art</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document cited for special reason other than those referred to in the other categories</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but on or after the priority date claimed</p> <p>"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance</p>		
<b>IV. CERTIFICATION</b>		
Date of the Actual Completion of the International Search <sup>1</sup>	Date of Mailing of this International Search Report <sup>1</sup>	
16 March 1982	26 MAR 1982	
International Searching Authority <sup>1</sup>	Signature of Authorized Officer <sup>19</sup>	
ISA/US	<i>Stuart R. Hecker</i>	